## Chapter 1. TOP\_DMAC Controller

### 1.1 Overview

The top\_dmac controller is a highly configurable, highly programmable, high performance, multimaster multichannel DMA Controller with AXI as the bus interface for data transfer.

### 1.2 Block Diagram



Fig. 1.1 top dma controller module block diagram

### 1.3 Features

■ Independent core, slave interface and master interface clocks

■ Up to two channels, one per source and destination pair   
■ Data transfers in one direction only (each channel is unidirectional)   
■ Up to two AXI master interfaces

■ Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers   
■ AMBA 4 AXI-compliant master interface  
■ AHB slave interface for programming the DMA controller

■ AXI master data bus width up to 128 bits (for both AXI master interfaces)

■ Independent control for endian scheme of linked list access on master interfaces

■ Channel locking support

❑ Supports locking of the internal channel arbitration for the master bus interface at different transfer hierarchy

■ DMA hold function

■ Multiple levels of DMA transfer hierarchy

❑ DMA transfer split into transaction, block, and complete DMA transfer levels